March 2026

HAL4SDV Newsletter 2

Hardware Abstraction Layer for a European Software Defined Vehicle Approach

HAL4SDV aims to pioneer innovative methods, technologies, and processes for series vehicle development beyond 2030. This ambitious project is driven by anticipated advancements in microelectronics, communication technology, software engineering, and AI to tackle Systems, Safety, Security, and Software.

The project's objectives are comprehensive and far-reaching, spanning the unification of software interfaces, creation of a robust hardware abstraction framework, facilitating of Over-The-Air (OTA) updates, designing of advanced platform architectures, and the provision of essential development tools. These objectives are pivotal in ensuring the agility and adaptability of the European automotive industry to meet the demands of the future.

Project coordinator:
Andreas Eckel
TTTech Computertechnik AG

Duration:
36 months

Number of partners:
59

Total budget:
€ ~64,5M

Number of countries:
11

EU contribution:
€ ~17,8M

Project start:
2024 04 01

About HAL4SDV

In line with the EU Strategic Research and Innovation priorities on Electronic Components and Systems, key European industrial companies, research organizations, and academic organizations from eleven countries started a three-year project to pioneer innovative methods, technologies, and processes for series vehicle development beyond 2030.

Mission

The HAL4SDV project's mission is to advance European solutions in software-defined next-generation vehicles. By focusing on unifying software interfaces and development methodologies, HAL4SDV will enable software configuration that abstracts from vehicle hardware, paving the way for a "software-defined vehicle (SDV)" approach for both safety critical and non safety critical applications in future vehicles.

Vision

This project is ready to shape the future of mobility, secure Europe's leadership in the automotive sector, and drive progress toward a more connected, efficient, and environmentally conscious future in the automotive sector. Moreover, it responds to the pressing need for Europe to invest massively in technological leadership in the automotive domain, ensuring the region's future growth and prosperity.

Beyond technological innovation, HAL4SDV underpins Europe's automotive industry, sustains its competitive edge, accelerates green and digital transitions, both fostering collaboration and promoting sustainability across the automotive ecosystem.

Technical Achievements in Transversal Activities, Year 2

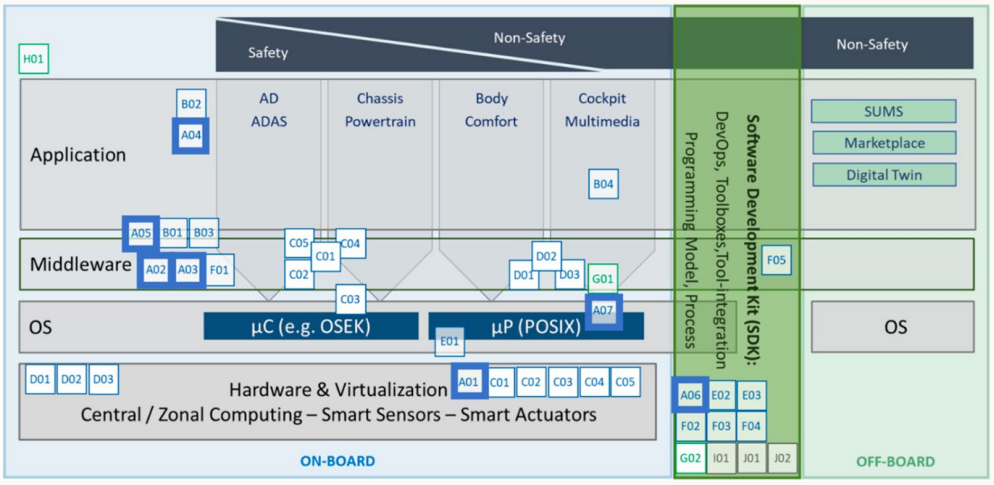
TA-A HW/SW Abstraction

Leader: Mercedes Benz AG

TA-A works on the decoupling of the OS layer from the underlying hardware, enablement of mixed-criticality systems (e.g., on multicore HPC processors), and increased safety and security mechanisms to meet relevant regulations and standards, e.g., ISO 26262 or Cyber-Security Resilience Act. In the first two years, the safety and non-safety requirements related to TA-A SW/HW Abstraction have been collected by the partners and selected building blocks have already been developed or are under development. These building blocks form our HAL4SDV reference architecture that serves as foundation for the realization our collaborative use cases. Some highlights of building blocks created in TA-A include:

- Open Vehicle API (Partner: ZF): With their openly available vehicle API, ZF provides a valuable foundation for HAL4SDV, abstracting specific OEM or supplier interfaces. By using the open vehicle API, software development can be accelerated, and a higher level of quality can be achieved.
- TSN simulation and scheduling (Partner: TU/e): With the TSN simulation and scheduling tool, TU/e provides a building block to simulate complex networks inside a vehicle. By using the simulation tool, bottlenecks, potential errors, and other metrics can be detected in an early stage of development.
- CARISMA – Car-integrated Services Mesh Architecture (Partner: MBAG): CARISMA provides a new kind of architecture for integrating services within in-vehicle architectures, enabling their loose coupling. CARISMA is fully open-source and available as building block on the company GitHub account of MBAG.
- XEN Hypervisor – A promising open-source approach for the virtualization of automotive use cases (Partner: VIF): The XEN hypervisor provides an open-source building block that is specifically re-designed to host automotive safety-critical applications.

Figure 1.
Figure 1 TA-A overview.



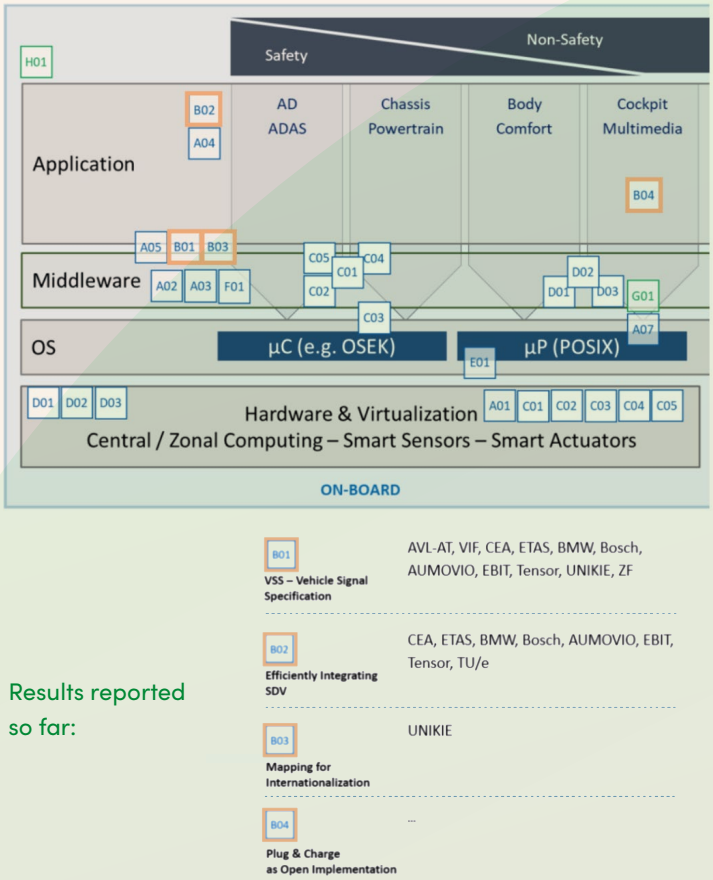
TA-B

Leader: ETAS GmbH

In year 2 results for the following Development Topics were discussed and collected in TA BB-B:
- VSS vehicle specification,
- Efficiently integrating SDV,
- Mapping for internationalization (also related BB-A).

BB-B looks at vehicle level abstraction w.r.t. VSS and related requirements, analysis and blue-print system implementations, looking for harmonization of approaches (i.e.: Eclipse KUKSA, ...) and API handling effort reduction managing complexity. Furthermore, it collects the required APIs and interfaces for both non-safety-relevant and safety-relevant applications.

The partners meet on a bi-weekly base, one schedule per month is focussing on "tech talks". This is the room for the partners to show and discuss their specific results in the partner forum. Detailed presentations on their approaches working with VSS were already given by: AVL-AT, VIF, CEA, ETAS, BMW, Bosch, AUMOVIO (formerly CONTI), EBIT, Tensor, UNIKIE, ZF, TU/E.



Results reported so far:

B01 VSS – Vehicle Signal Specification	AVL-AT, VIF, CEA, ETAS, BMW, Bosch, AUMOVIO, EBIT, Tensor, UNIKIE, ZF
B02 Efficiently Integrating SDV	CEA, ETAS, BMW, Bosch, AUMOVIO, EBIT, Tensor, TU/e
B03 Mapping for Internationalization	UNIKIE
B04 Plug & Charge as Open Implementation	...

Figure 2.
TA-B overview.

TA-D Cyber Security Orchestration

Leader: TTTech Auto AG

TA BB D consists of the development topics dealing with general aspects of security in SDV context. Specifically, it focuses on security threat analysis, on-board security service gateway software and cloud connectivity: security service integration to on-board integration software environment. Last year work on BB TA D progressed from conceptual requirements toward prototypes, functional software components, and security methodology development. For the security gateway, multiple functional scenarios are starting, and a security testing catalogue that will support future testing frameworks and guide SDV security architecture is planned. Also, the methodological multilevel approach is included. Further, we advanced research on agentic AI approaches for SDV cybersecurity, combining complementary AI models with model-driven engineering for complex defense and attack planning. An initial prototype includes components for generating system models, translating security rules into constraints, scanning source code and deployments, analyzing logs for anomalies, and generating defensive actions.

We continued work on AI-based threat detection and energy profiling of lightweight protocols, with integration into use cases under discussion. The collaboration on remote operation is ongoing and should be extended during talks with Skoda. On the hardware security module abstraction the use use case is being developed and is with multiple plartners. The work on penetration test generation for UC3, including OTA analysis using ThreatGuard is progressing well. RES advanced its work with 3DS and will apply its multilevel approach to UC5 and the security gateway.

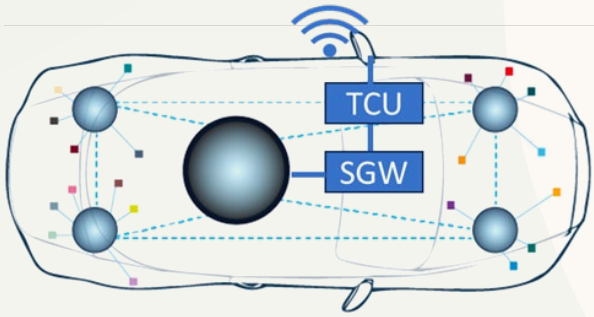


Figure 3.
Security Gateway.

TA-E Development Process Tool

Leader: Valeo FR

During year 2, TA-E partners focus shifted toward enhancing the HAL4SDV platform through automation, real-time monitoring, and advanced safety-critical language assessments.

Key Technical Contributions

The partners focused on five primary pillars to streamline the SDV development lifecycle:
- **GenAI-Powered Engineering Workflows:** Implementing automated translation from requirements to test cases to significantly reduce manual verification efforts.
- **Real-Time Performance & Monitoring:** Development of specialized tools to provide deep visibility into system latency and resource utilization.
- **Quality and Resource Management:** Deployment of an Orchestrator framework. This uses component models and mapping tools to balance application quality-of-service with available platform resources.
- **Secure Programming (Rust):** A deep-dive evaluation of Rust's memory safety features, specifically analyzing their impact on Worst-Case Execution Time (WCET) guarantees.
- **AI-Driven Open-Source Qualification:** Investigating how AI can accelerate the compliance and qualification process for open-source components within automotive standards.

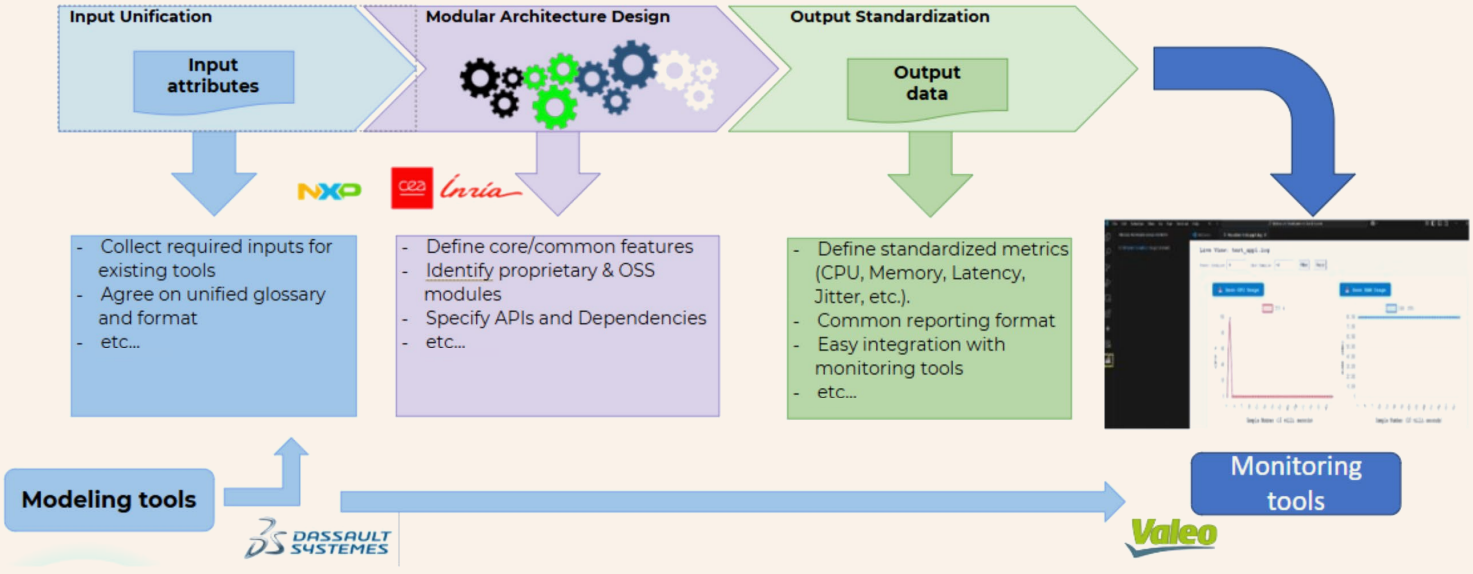


Figure 4.
Tools Interoperability for System Performance Analysis & Monitoring.

TA-F Integration, Testing, Simulation, Tools

Leader: AVL List GmbH

TA-F's work on Integration, Testing, Simulation, and Tools drives a unified approach to Verification & Validation for SoftwareDefined Vehicles. Partners collaborate on AIbased test generation from requirements, using machine learning and LLMs to accelerate coverage and identify gaps early. Distributed and virtual testing environments (SiL, HiL) enable scalable, repeatable validation of complex SDV functions. We investigate how certification can be supported by simulation evidence to support regulatory approval. Monitoring, observability, and tracing improve transparency across distributed components, complemented by source code optimization and timing analysis to meet realtime constraints. CI/CT/CD pipelines tailored for automotive workflows ensure continuous, standardscompliant integration and testing. Architecture work is done on defining new interfaces and APIs, like a neutral configuration layer for virtual test environments. V&V is supported by ModelBased Systems Engineering to maintain consistency across requirements, design, and tests. Enhanced simulation tools, guidelines, and development processes help partners integrate, test, validate, and verify SDV systems efficiently, forming a robust foundation for safe and reliable automotive software.

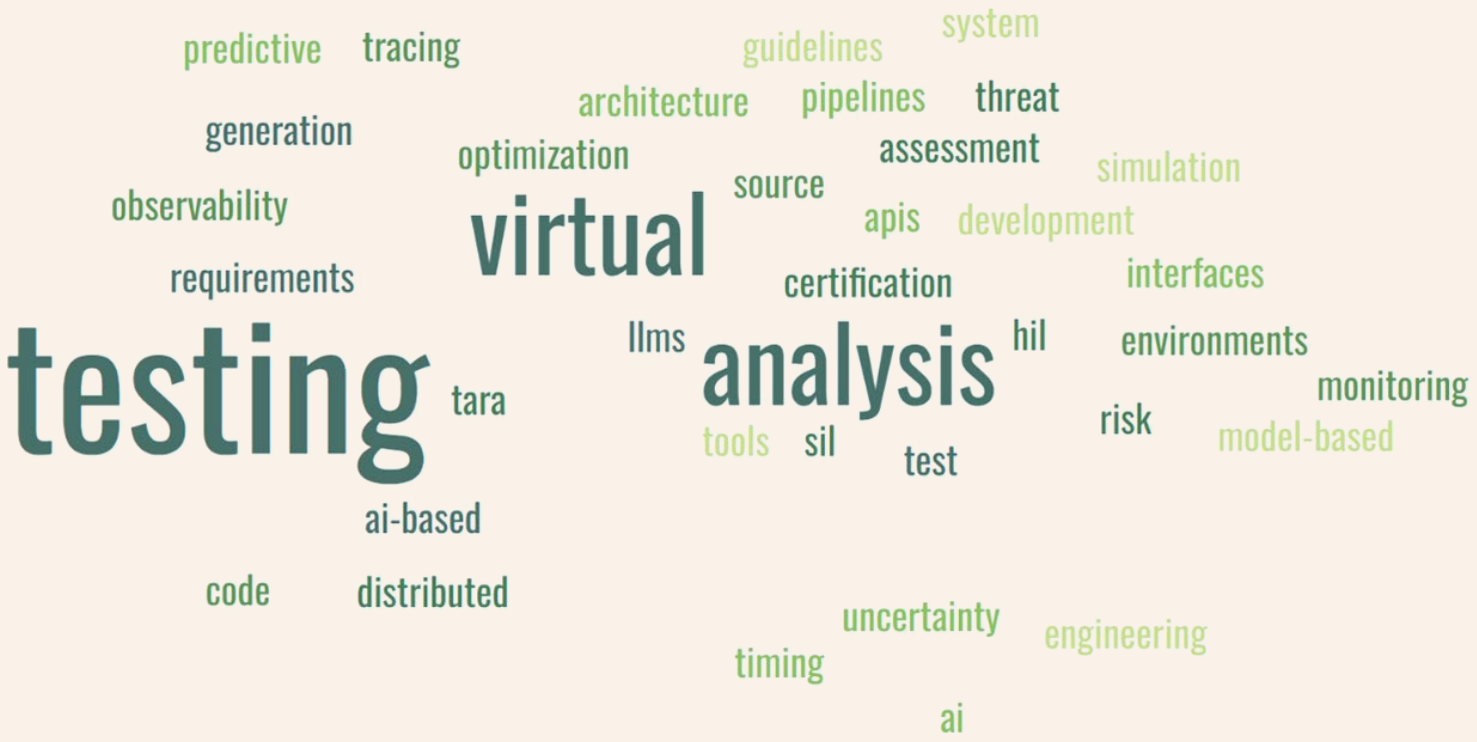


Figure 5.
TA-F Focus Areas.

Technical Achievements in Use Cases

UC1 Chassis/Powertrain domain

Leader: ZF

During the 2nd year of the project significant progress was made for getting the bench setup and vehicle demonstrator prepared showcasing a mixed-critical architecture on a HPC. The major scope was here in modeling and integration of the platform software (Drivers, OS, Eclipse Open Vehicle API) and the Low-Speed Driving Characteristic (LSDC) function.

- Analyzing requirements to satisfy the assumption of use in a safety application on the OS.
- Definition of split for the LSDC function targeting a mixed criticality application.
- Modeling the system architecture in CAMEO Systems Modeler outlining the HPC architecture and function allocation with interfaces.
- Bring up of HPC with OS and Eclipse Open Vehicle API framework and necessary bus interface (CAN) drivers.
- Performance measurements on HPC for analyzing timing constraints in non-safety configuration.
- Initial setup of a DevOps pipeline enabling packaging for OtA updates.
- Definition of function interfaces following the Covesa-VSS and description of function properties in a description model.
- Integration of LSDC function as a component into the Eclipse Open Vehicle API framework.
- Identification and conversion of logfile recording from SofDCar project for doing smoke tests after integration.

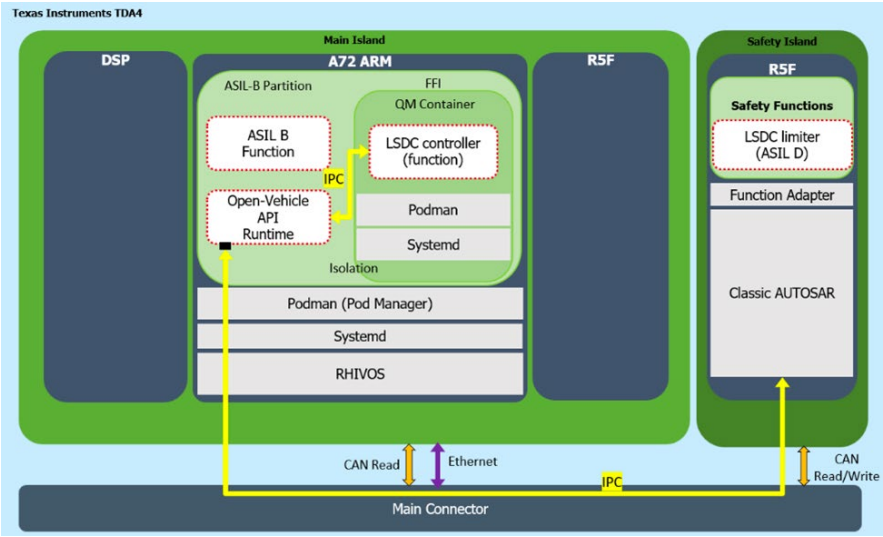


Figure 6.
HPC architecture with Open-Vehicle API and LSDC in safety allocation.

UC3 ADAS/Autonomous Driving

Leader: Technical University of Munich

In Project Year 2, the consortium substantially strengthened the technical depth and maturity of the project by expanding the demonstrator portfolio to eight lab-based and vehicle-level demonstrators and involving additional partners. Together, these demonstrators cover a broad range of ADAS-oriented hardware abstraction challenges, including GenAI-assisted abstraction layers, model-driven architecture and timing analysis, mixed-criticality virtualization, and automated software update mechanisms.

Significant progress was achieved in laboratory environments, where demonstrators validated hypervisor-based isolation, WebAssembly application isolation on safety MCUs, and real-time ADAS pipelines with improved traceability between models and implementation. Several use cases now execute in real time across heterogeneous platforms, from development PCs to embedded ARM systems and virtual prototypes, enabling automated analyses of consistency, schedulability, causality, and end-to-end latency.

Vehicle demonstrators focused on software portability, performance and safety evaluation of virtualization solutions, and OTA-ready system evolution. The SAE Level-4 open-road demonstrator delivered an integrated automated driving stack featuring sensor abstraction, LiDAR-agnostic perception, containerised core modules, and data-centric middleware evaluation toward final integration.

In parallel, the emergency braking demonstrator validated LLM-enabled hardware abstraction and automated system extension, supported by scientific publications and enhanced timing analysis tooling. Overall, Year 2 consolidated core technologies, demonstrated feasibility in realistic environments, and laid a robust foundation for large-scale integration and validation in the final project phase.

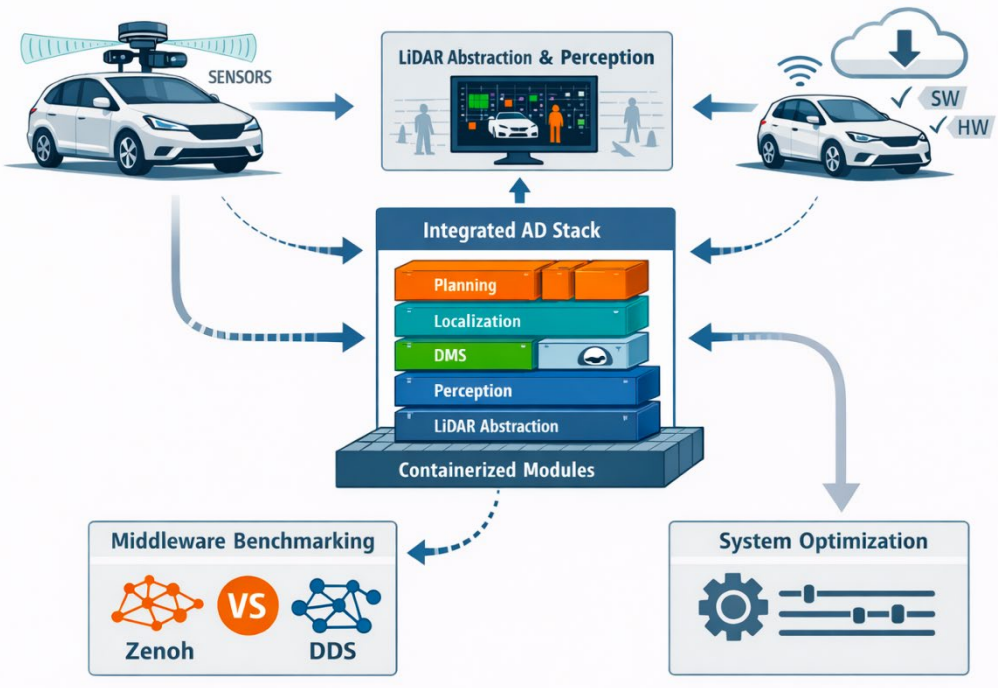


Figure 7.
SAE L4 Automated Vehicle Driving in Open Roads – integrated stack so far.

UC4 Execution Environment

Leader: AUMOVIO

SDV NeXT Experience: End to End Federated Software-Defined Vehicle

AUMOVIO's NeXT Framework envisions an end-to-end solution for Software-Defined Vehicle (SDV) ecosystem enabling safe and secure orchestration based on our work in Gaia-X 4 AGEDA with cloud-native tech, Self-Sovereign-Identity (SSI), Verifiable Credentials (VCs), and mixed-criticality execution management.

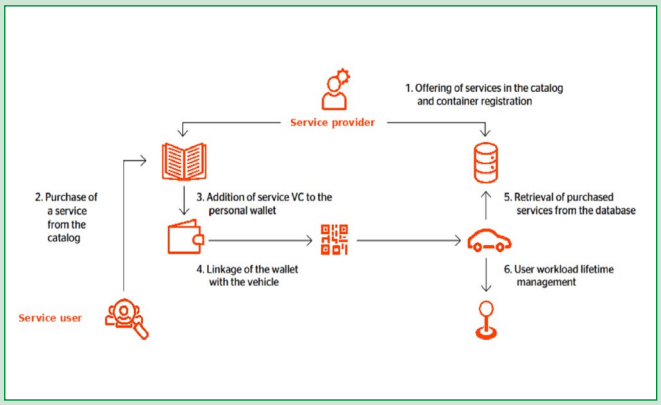


Figure 8.
SDV NeXT Experience interactions.

The SDV NeXT Experience highlights key pillars of software-defined mobility, including:

- **OEM governance,** multiple partners contribute software assets accompanied by digital manifests that formally describe resource requirements, safety-aware runtime dependencies, and requested data access. Enabling transparent governance, controlled deployment, and scalable ecosystem collaboration.
- **User agency and data sovereignty,** End users personalize in-vehicle experience where trust is assured by cryptographic mechanisms supporting vendorindependent digital identity, data sovereignty and interoperability across organizational boundaries.

A live demo was delivered at HAL4SDV consortium meeting in Munich (25 Feb 2026) featuring open-source components including Ankaios, Kuksa.val, walt.id, and Zenoh.

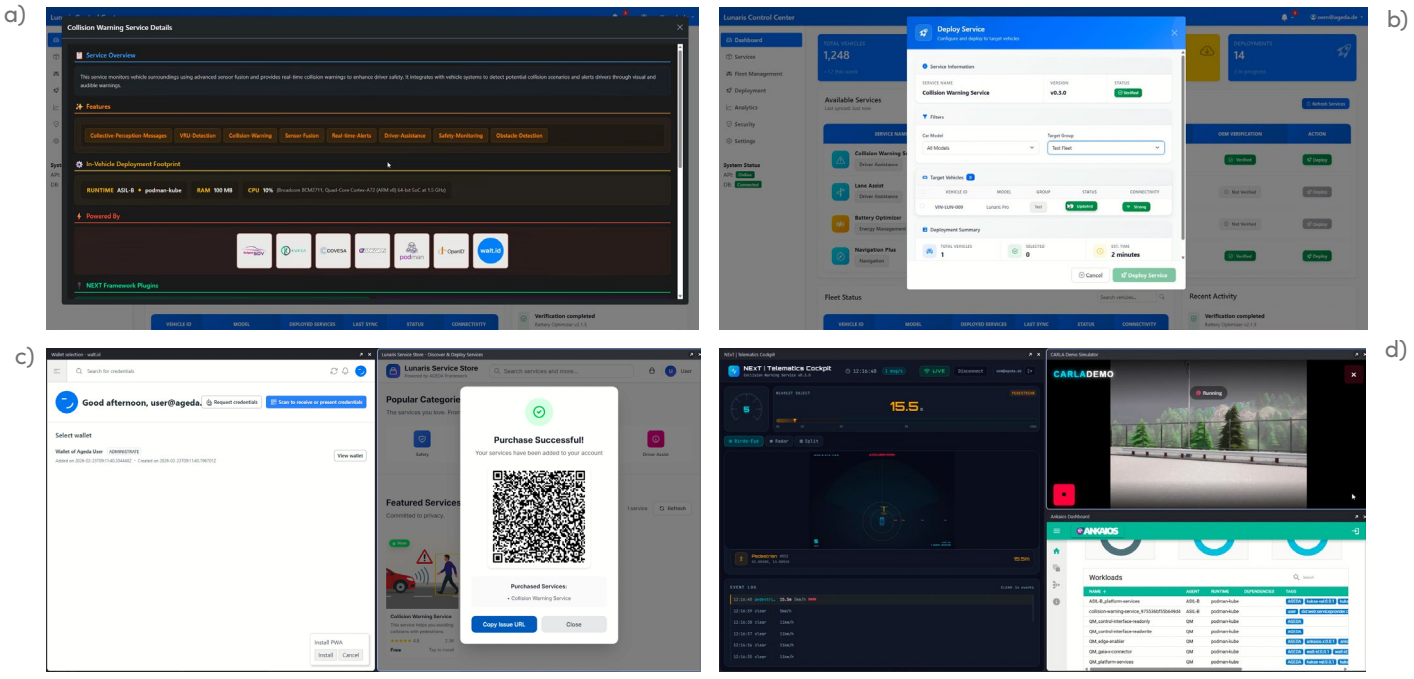


Figure 9.
Collision Warning Service demonstrator illustrates the full lifecycle of introducing new in-vehicle functionality – Clockwise (a) Software asset description and requirements (b) OEM marketplace release (c) user-controlled activation via a personal SSI wallet (d) VC-based, safety aware runtime orchestration on virtual ECUs.

UC4 Execution Environment (continued)

Leader: AUMOVIO

vSDV Composer is a cloud-based platform for software development and virtualization, enabling teams to advance SDV software development ahead of physical hardware availability through virtualized environments. vSDV Composer accounts are available to HAL4SDV partners for evaluation. Example setups based on generic Ubuntu and Android platforms were presented at TA-F and TA-B meetings. Further developments presented at the HAL4SDV consortium meeting in Munich (25 February 2026) include:

- An Ubuntu-based setup with successful ROS2 integration, validating TimeSync support via SilKit with PTP, enabling further analysis in collaboration with TU Eindhoven.
- Demonstration of GPU support, full functionality using VirtIO and passthrough modes currently under analysis.

An S-CORE reference integration on EB Linux is planned to be available during March '26.

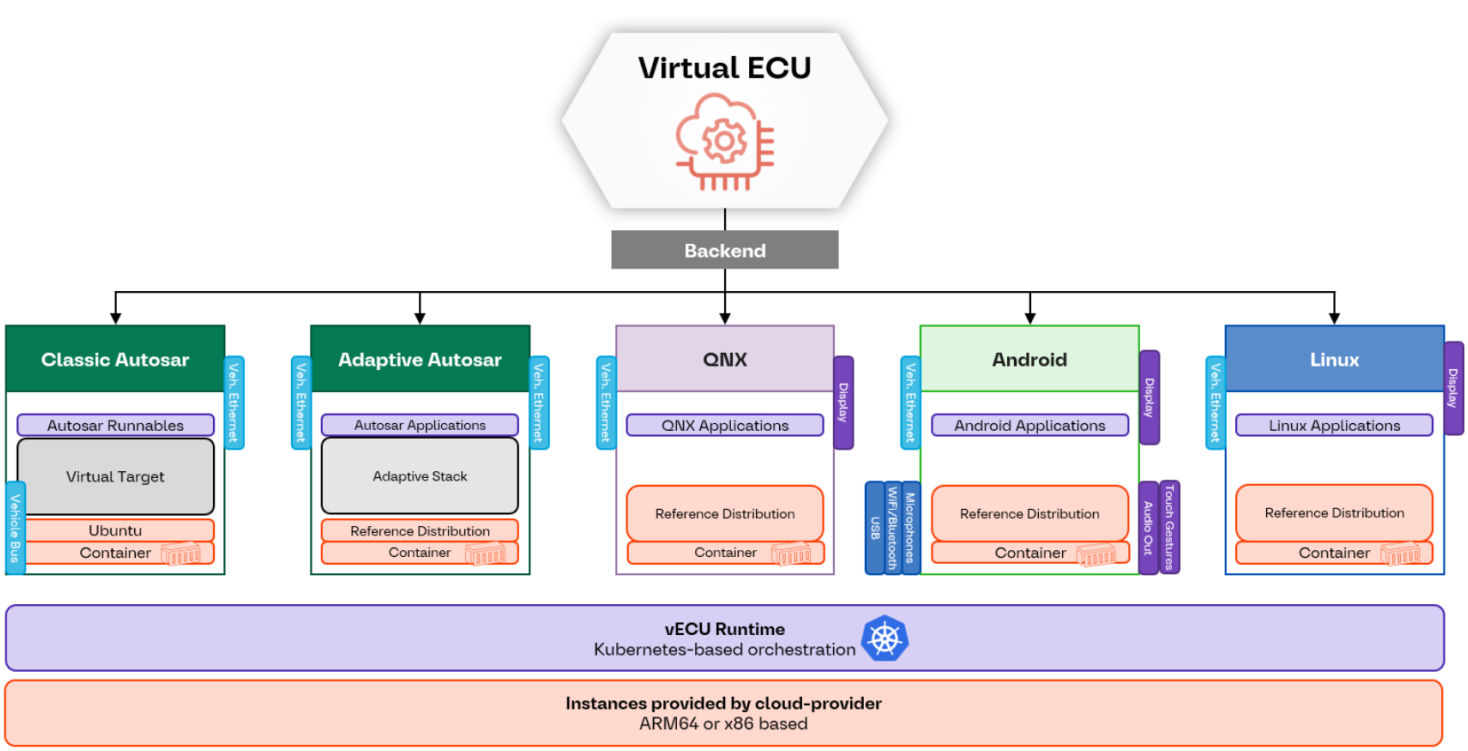


Figure 10.
Example vECU with multiple Partitions on different SOCs.

UC5 Security Measures Demonstrator

Leader: TTTech Auto AG

Use Case 5 moved from conceptual planning into the design and initial implementation phase, with the team focusing on defining the Security Gateway services and detailing the functional scenarios that will guide the demonstrator's development. Building on the architectural foundations established earlier, the work concentrated on specifying the roles of the security, update and monitoring services, as well as refining how internal and external networks interact in secure SDV environments. The demonstrator setup was prepared, including the gateway hardware, cloudsimulation environment and the ECU used for showcasing secure OTA behaviour, enabling the team to start integrating the software framework.

A major activity this year was the formulation of routing, diagnostic and security scenarios—such as encapsulation, mirroring and secure update flows—which form the basis for upcoming evaluation. With service definitions, interfaces and testing plans now aligned with partners, the project is entering the phase where implementation of these scenarios is begin, paving the way toward demonstrating robust protection during OTA updates.

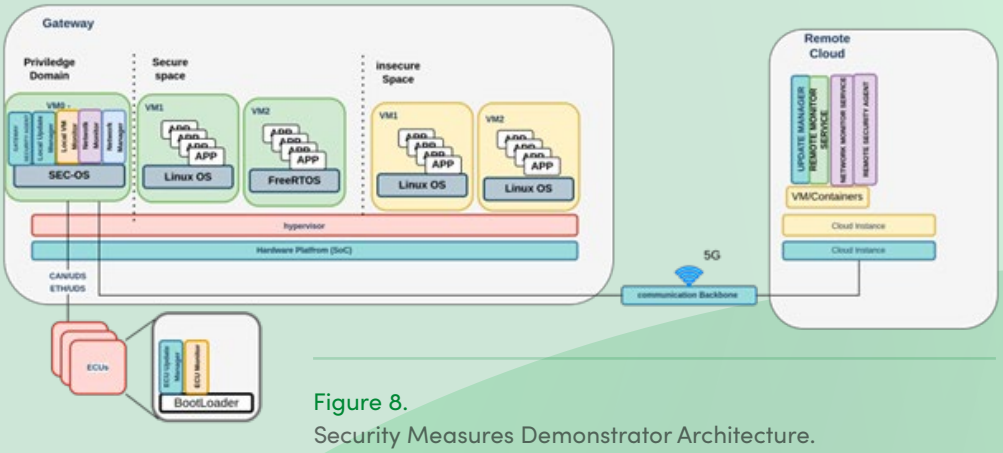


Figure 8.
Security Measures Demonstrator Architecture.

UC6 Mixed Criticality

Leader: TTTech Auto AG

Use Case 6 progressed from architectural concepts to the first concrete steps toward a mixedcriticality onboard integration platform capable of safely running realtime and noncritical workloads on shared automotive hardware. Work focused on detailing the platform architecture on the NXP S32G evaluation boards, defining the software stack across MPU and MCU, and specifying scheduling, orchestration and timetriggered execution mechanisms. The team refined how mixedcriticality applications are planned, synchronized and executed, preparing scenarios that demonstrate deterministic behaviour even under high system load. Computation chains, tracing features and timetriggered scheduling were analyzed to ensure that realtime tasks can be guaranteed and monitored across heterogeneous compute units. A simulationbased demonstrator environment was prepared to show predictable execution during automateddriving workloads. With service definitions, scheduling methods and scenario descriptions now established, the use case is entering the implementation phase, including further scenario development and investigations of extended environments and crossusecase integration.

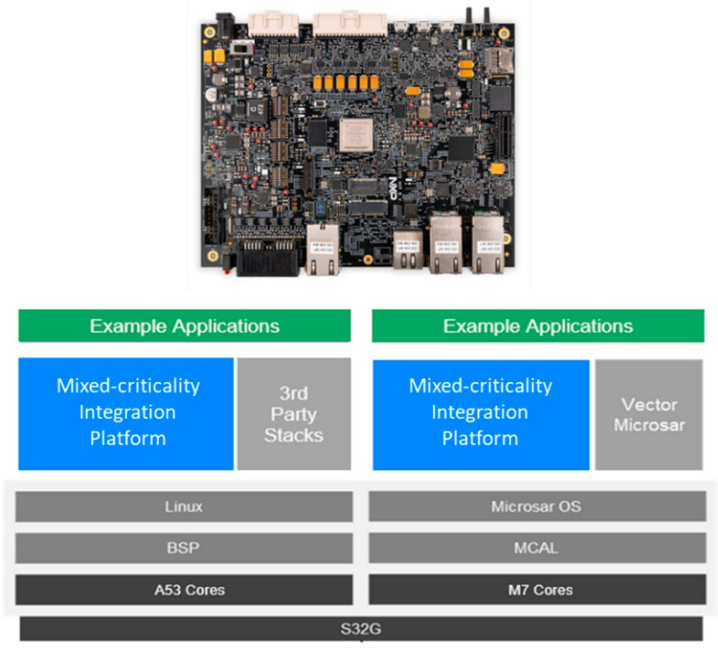


Figure 11.
Mixed Criticality Demonstrator Architecture.

UC7 TSN Communication for Mixed Criticality Computation Demonstrator

Leader: TTTech Computertechnik AG

In UC7, we defined the demonstrator architecture. The distributed system design is based on the S32G Safety microcontroller and NXP S32G MPUs, supporting object detection and vehicle control. Multiple applications run across two software environments (Linux and Microsar). Communication is enabled through DDS on the MPU side and Zenoh on the MCU side, connected via a Zenoh DDS bridge. The MCU stack incorporates Zenoh Pico and a Gateway enabling communication with Autosar Classic software components.

The network configuration supports importing or building topologies via draganddrop or a tablebased editor, defining talkers/listeners and stream constraints, and generating IEEEcompliant GCL schedules through the integrated network configuration engine. Incremental rescheduling allows adding devices or streams without disrupting active setups. The planning framework supports latency, bandwidth, and mixed TSN/nonTSN requirements, exporting NETCONF/YANG configurations directly to devices. We are now planning the setup phase and intend to involve NXP as a collaboration partner.

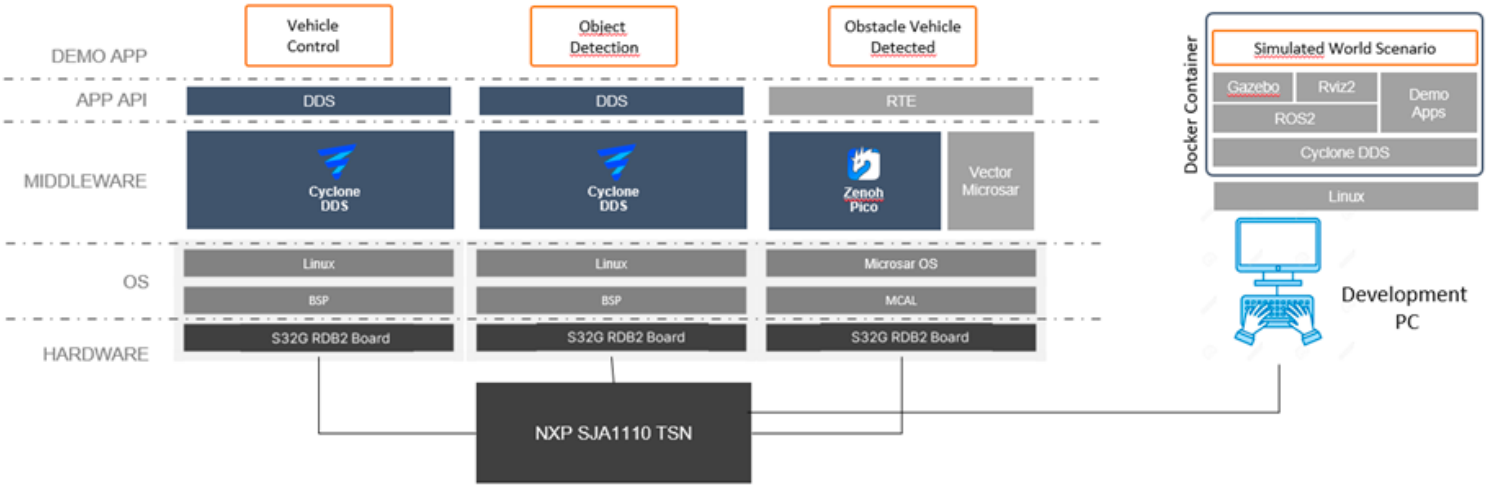


Figure 12.
Demonsrator Architecture for the Moose Test.

Dissemination

The European SDV Ecosystem Summit 2025

On the 20th of May, 2025, Andreas Eckel, coordinator of the HAL4SDV project, took the stage at the European SDV Ecosystem Summit 2025, held in Munich. The event was organised by the FEDERATE project and hosted by Infineon Technologies AG. Bringing together more than 150 stakeholders from across the mobility, software, and semiconductor sectors, the summit fostered a strong spirit of collaboration—emphasising partnership over competition in shaping the future of software-defined vehicles (SDVs).

The day opened with welcome words of Oliver Höing, representing Germany's Ministry of Research, Technology and Space. This was followed by keynote speeches from Thomas Schneid, Senior Director Software, Partner & Ecosystem Management (Infineon Technologies AG), Markus Rettstatt (Mercedes-Benz Tech Innovation GmbH), and Max Lemke (DG-Connect, EC).

The programme continued with a series of technical and strategic presentations. Michael Paulweber provided an overview of the FEDERATE project and the SDVoF initiative, while Daniel Watzenig presented insights from the Scientific Board. Additional contributions included a presentation on the RIGOLETTO project by Knut Hufeld.

HAL4SDV was featured during a dedicated session on SDV projects, presented alongside the CODE4EV and Twin-Loop initiatives, highlighting ongoing efforts to advance Europe's SDV ecosystem.

A central theme of the summit was addressing fragmentation within the SDV sector. Discussions focused on the need to build an integrated European technology stack—spanning semiconductors, system software, and open-source middleware. Participants agreed that a unified European approach is essential to deliver scalable, sustainable, and globally competitive mobility solutions.

Figure 13.
HAL4SDV at The European SDV Ecosystem Summit 2025.

The Autonomous Main Event 2025

This year's Autonomous main event marked the fifth anniversary of the Spotlight Session "From Concept to Reality: Enabling Safe, Trustworthy, and Software-Defined Autonomous Systems with European Innovation," hosted by Andreas Eckel (TTTech), coordinator of HAL4SDV. The session showcased Europe's strong leadership in advancing safe and secure software-defined autonomy, clearly demonstrating how European innovation is bridging the gap between cutting-edge research and real-world deployment. A key outcome was the reinforcement of a holistic approach to safety and security, integrating functional safety, cybersecurity, and overall trustworthiness as essential pillars for the scalable roll-out of autonomous systems across domains.

The workshop also emphasized the importance of cross-industry collaboration in building a robust European ecosystem capable of supporting autonomous mobility at scale, while providing actionable perspectives relevant to OEMs, Tier 1 suppliers, and regulatory stakeholders. This year's edition once again brought together leading European innovation projects—Shift2SDV (Michael Karner), ShapeFuture (Gorge Dimitrakopoulos), and EdgeAITrust (Georg Stettinger)— highlighting complementary efforts across the value chain. In addition, the participation of European Commission and CCAM Association representatives further strengthened the strategic alignment between research, industrial priorities, and policy: Stefan Bogensberger (DG CNECT) presented the Industrial Action Plan for the European automotive sector, while Dr. Stephane Dreher (Head of CCAM) shared the Status and Outlook of CCAM R&I. Collectively, these contributions underlined Europe's momentum in driving the development of safe, secure, and trustworthy autonomous systems, from innovation and validation to tangible deployment.

Figure 14.
Spotlight Session at the Autononous Main Event.

EFECS 2025

On the 3rd-4th of December 2025, the HAL4SDV project was showcased at EFECS 2025, the premier European forum dedicated to advancing the growth and innovation of the electronic components and systems (ECS) sector. Held in Malta, the event brought together approximately 700 policymakers, industry leaders, and researchers from across Europe, reaffirming its role as a key platform for shaping the continent's ECS agenda.

This year, HAL4SDV featured prominently at the Chips JU projects exhibition, where project coordinator Andreas Eckel delivered a project pitch highlighting the initiative's mission: to develop a unified Hardware Abstraction Layer that enables safe, secure, and scalable development for software-defined vehicles. Several project partners were present on-site, engaging in in-depth discussions on the future of automotive architectures, interoperability challenges, and Europe's pathway toward more flexible vehicle software ecosystems. Interactions with aligned initiatives further strengthened collaborative opportunities across the SDV landscape.

As in previous years, EFECS 2025 offered a rich programme of insightful presentations, providing attendees with a deep understanding of the Chips JU programme and its approach to addressing Europe's most pressing technological and economic challenges. The event also offered valuable networking opportunities, connecting participants with key stakeholders and the broader ECS community, and unlocking new avenues for collaboration and innovation.

Figure 15.
HAL4SDV at EFECS2025.

HiPEAC 2026

On the 27th of January, 2026, HAL4SDV project was presented at HiPEAC2026 conference in Krakow, Poland. HAL4SDV coordinator Andreas Eckel represented the project at the 14th edition of the Mixed-Criticality Systems (MCS) Workshop, co-organized by IKERLAN, Barcelona Supercomputing Center, and German Aerospace Center (DLR). The session covered key topics such as Trustworthy AI, Software-Defined Vehicles, and safety and security in mixed-criticality and RISC-V platforms.

This workshop brought together academic and industrial experts who presented their work, progress, and approaches across 11 research projects: SHASAI, Capsul-IA, EdgeAI-Trust, SAFEXPLAIN, UP2DATE4SDV, HAL4SDV, CODE4EV, Shift2SDV, RIGOLETTO, ISOLDE Project and SMARTY.

Figure 16.
HAL4SDV at HiPEAC2026.

Also, the project was presented by Edin Arnautovic from TTTech Auto. HAL4SDV partner Harrison Kurunathan presented a poster summarising Instituto Superior de Engenharia do Porto's contributions across multiple building blocks of the HAL4SDV project.

The poster highlighted key research topics, including: Compiler-Integrated Schedulability Analysis, Resource-Efficient DAG Dcheduling, Authentication Trade-offs for Software-Defined Vehicles, Resource sharing Long Heterogeneous Platooning.

HiPEAC 2026 provided an excellent opportunity for networking, establishing new connections, and fostering cross-project collaboration. During the event, Harrison Kurunathan met Gregor Nitsche, representing the UP2DATE4SDV project, and discussed potential synergies with HAL4SDV as well as opportunities for further collaboration between the two projects. Following these discussions, Gregor Nitsche later joined a HAL4SDV meeting in Munich to continue exploring possibilities for cooperation.

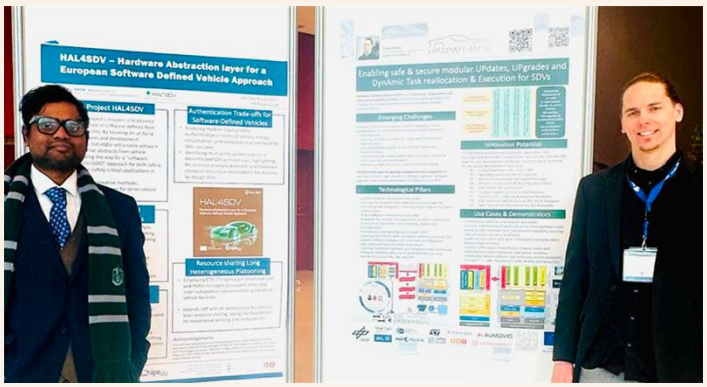


Figure 17.
Harrison Kurunathan (HAL4SDV) and Gregor Nitsche (UP2DATE4SDV) at HiPEAC2026.

RTR 2026

On the 10th-12th February, 2026, the HAL4SDV project was presented at RTR 2026 conference in Brussels. The coordinator, Andreas Eckel, presented HAL4SDV in the Parallel Session 31 "Software Defined Vehicles" moderated by Stefan Bogensberger, EC DG CNECT and Jean Baptiste Burtscher, Valeo. The co-presenters were Stefano Persi, MOSAICfactor, presenting 2ZERO Project TWIN-LOOP and Valentin Ivanov, TU Ilemnau presenting Code4EV. The session was closed after having a very interesting and lively discussion with highly ranked representatives from industry and academia, contributing from the side of the audience.

Figure 18.
HAL4SDV at RTR 2026.

SDV Breakfast

On the 17th February, 2026, HAL4SDV partners: University of Oulu, VAMOS Ecosystem, Unikie, and VTT organised an SDV Breakfast in Tampere, bringing together experts from across the mobility ecosystem. At the event, Ella Peltonen from the University of Oulu represented both the HAL4SDV and Shift2SDV projects, which play a key role in the development of European Software-Defined Vehicles.

The main purpose of the event was to explore how Software-Defined Vehicles are reshaping the automotive industry, how the landscape of software and hardware standards is evolving and, what new business opportunities may emerge in the European market as a result.

The event was hosted by Janne Uggeldahl from VAMOS Ecosystem – an innovation cluster focused on autonomous mobility in smart spaces. VAMOS connects OEMs, major automotive suppliers, and researchers to collaboratively develop the future of European SDVs.

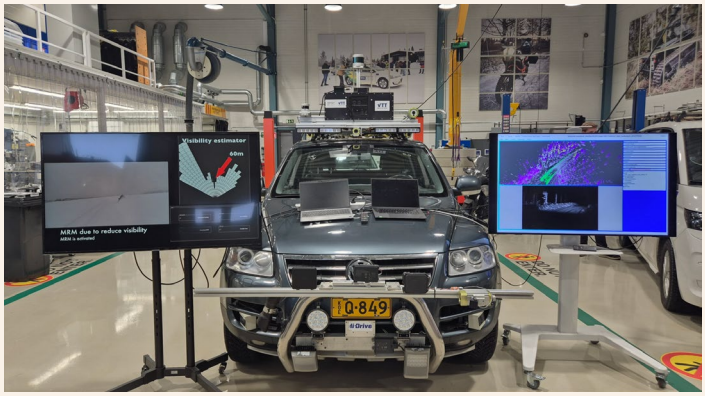


Figure 19.
SDV Breakfast in Tampere.

Partner Announcement

vSDV Composer – Exclusive for HAL4SDV partners!

AUMOVIO invites HAL4SDV partners to explore vSDV Composer - smart workbench for software development and virtualization. The vSDV Composer combines virtualized hardware, an integrated development environment, a collaborative workspace, and tailored services — all designed to empower software development teams through advanced virtualization.

The vSDV Composer is a cloud-based framework for:

- Replacing real hardware by using digital twins.
- Optimizing resource allocation by reducing investment in hardware tools.
- Developing software ahead of hardware availability.
- Setting up development environments fast and at scale.

HAL4SDV partners can now get dedicated access to explore vSDV Composer and experience the advantages of virtual development. Whether you want to accelerate your demonstrator development before physical hardware is available or build a fully virtual showcase, you can use vSDV Composer as part of your partnership benefits.

Register here!

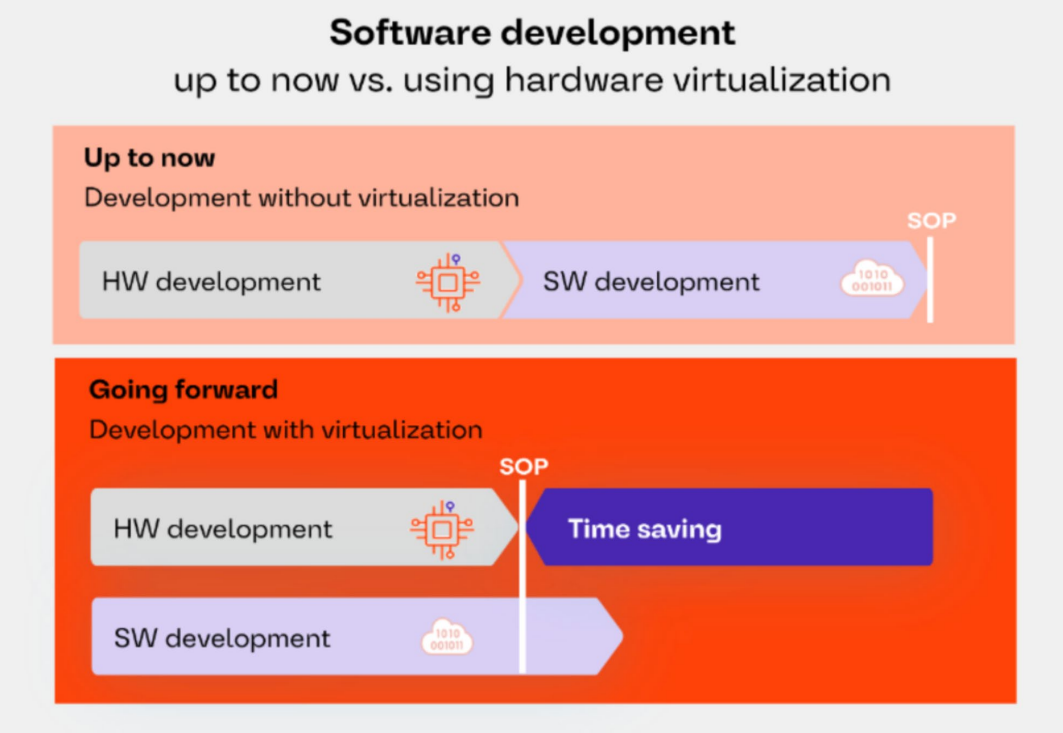


Figure 20.
Accelerated Software Development.

Consortium & Funding

Partners

Associated Partners

About Chips Joint Undertaking:

Chips Joint Undertaking is a collaborative initiative between the European Commission and the European industry, dedicated to advancing research and innovation in the field of microelectronics. By fostering partnerships and funding groundbreaking projects, Chips JU aims to strengthen Europe's position in the global semiconductor landscape.

Acknowledgment:

HAL4SDV is supported by the Chips Joint Undertaking and National Authorities under grant agreement n° 101139789.

Disclaimer:

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Co-funded by the European Union